BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

REMARKS

Entry of this amendment in this application, and favorable reconsideration of this application based on that amendment and these following remarks, are respectfully requested.

Claims 1, 2, 7, 9 through 12, and 14 through 19 remain in this case. Amendment to claims 1, 2, 7, 12, and 15 through 19 is presented.

The specification was objected to because of the presence of the attorney docket numbers in the first paragraph on page 1, and because a comma was missing in the second full paragraph of page 14, both as amended. Amendment is presented to these two paragraphs to correct these errors, as required by the Examiner. No new matter is presented by this amendment. Applicants respectfully submit that this amendment to the specification overcomes the bases of objection raised by the Examiner.

Claims 2, 12, and 17 were objected to for various informalities. Amendment to claims 2, 12, and 17 is presented above as required by the Examiner. Applicants therefore respectfully submit that proposed amended claims 2, 12, and 17 overcome the bases of objection raised by the Examiner.

Claims 7, 12, and 14 through 17 were finally rejected under §102(a) as anticipated by the Intel reference[1]. The Examiner asserted that the Intel reference teaches all elements of these claims. Claims 1, 2, 9, 10, 18, and 19 were finally rejected under §103 as unpatentable over the Intel reference in view of the Hennessy et al. reference[2]; the Examiner asserted that the Intel reference teaches all the elements of the claims except a plurality of pipeline phases, but that the plurality of pipeline phases is taught by the Hennessy et al. reference and would have been obviously combined with the Intel teachings to increase processor throughput.[3] Claim 11 was finally rejected under §103 as unpatentable over the Intel and Hennessy et al. references, further

---

[1] *IA-64 Application Developer's Architecture Guide*, (Intel, May 1999).
[2] Hennessy and Patterson, *Computer Architecture – A Quantitative Approach* (2d ed., 1996).
[3] Office Action of May 28, 2004, page 12, ¶17.

in view of the Haataja reference[4]; the Examiner asserted that the Intel and Hennessy et al. references, applied as discussed above relative to claim 1, still lack explicit teachings that the digital system is a cellular telephone, but that such teachings are provided by the Haataja reference and would have been obviously combined to reach the claim, to increase system functionality.[5]

Amendment is presented to claim 1 to clarify its patentability over the prior art. Proposed amended claim 1 now recites that the byte intermingling circuitry places non-contiguous data from selected fields of the first source operand contiguously in a most significant portion of the destination operand, and places non-contiguous data from selected fields of the second source operand that are at the same positions as the selected fields from the first source operand, contiguously in a least significant portion of the destination operand. The specification clearly supports this proposed amendment to claim 1, for example by the examples of the PACKH4 and PACKL4 instructions in which non-contiguous data from the source operands are contiguously placed into the destination operand as claimed.[6] Accordingly, no new matter is presented by this proposed amendment to claim 1.

Claims 18 and 19 are also proposed to be amended, for consistency with the proposed amendment to claim 1, upon which they depend.

As previously argued, the digital system of proposed amended claim 1 provides important advantages, particularly by way of the byte intermingling recited in the claim that enables the definition of a new instruction. As disclosed in the specification,[7] this instruction simplifies the manipulation of packed data in a microprocessor, thus improving the overall performance of the processor.

Applicants respectfully submit that, upon entry of the amendment to claim 1, it and its dependent claims will be patentably distinct over the prior art of record.

---

[4] U.S. Patent No. 6,137,836, issued October 24, 2000, to Haataja.
[5] Office Action, *supra*, pages 15 and 16, ¶24.
[6] Specification of S.N. 09/702,405, at page 26, Table 9; page 30, lines 9 through 12 and lines 17 through 20.
[7] Specification, *supra*, page 24, line 23 through page 25, line 5.

In the final rejection of claim 1, the Examiner asserted that the Intel reference discloses, relative to its "mix 1.l" instruction, the placing of non-contiguous data from selected fields (7, 5, 3, and 1) of one operand to a most significant portion of the destination operand *rl* (fields 7, 5, 3, and 1), and the placing of non-contiguous data from selected fields of a second operand, in the same position (fields 7, 5, 3, 1), to a least significant portion of the destination operand *r1*.[8] The Examiner asserted that the most significant portion of the destination operand *r1* comprises its upper seven fields (fields 7 through 1) because these seven fields do not include the least significant field, and that the least significant portion of the destination operand *r1* comprises its lower seven fields (fields 0 through 6) because these seven fields do not include the most significant field.[9]

Applicants do not agree with this interpretation of the most significant and least significant portions of the destination operand, and do not agree that the Intel reference teaches the placing of data from the first and second operands into the most significant and least significant portions of a destination operand. But claim 1 is proposed to be amended to overcome even the Examiner's interpretation of the reference, in order to advance the prosecution of this case.

As mentioned above, proposed amended claim 1 now requires that the non-contiguous data from selected fields of the first source operand are placed contiguously in a most significant portion of the destination operand, and that the non-contiguous data from selected fields of the second source operand, at the same positions as those in the first source operand, are placed contiguously in a least significant portion of the destination operand. The Intel reference fails to teach this contiguous placing of the non-contiguous data of the respective source operands. Rather, as is clearly shown in the reference,[10] the data from source operands *r2* and *r3* are placed in destination operand *r1* in an interleaved fashion relative to one another. Accordingly, the Intel reference therefore falls short of the requirements of proposed amended claim 1, even if interpreted in the manner presented by the Examiner in the Office Action.

---

[8] Office Action, *supra*, page 11, ¶1(d).
[9] *Id.*
[10] Intel, *supra*, Figure 7-23, page 7-117.

The Hennessey and Haataja references lack teachings regarding the contiguous placing of data by byte intermingling circuitry in the manner now recited by proposed amended claim 1. Accordingly, Applicants respectfully submit that the combined teachings of the applied references fall short of the requirements of proposed amended claim 1.

Applicants further respectfully submit that there is no suggestion from the prior art to modify these combined teachings in such a manner as to reach the requirements of proposed amended claim 1. It is instructive, in this regard, that the Intel reference, with all of its combinations of "mix" and "mux" instructions, fails to provide the byte intermingling recited by proposed amended claim 1. And the Hennessey and Haataja references are in no way concerned with specific byte intermingling operations, as evident from their contents. Especially considering the advantages provided by the system of proposed amended claim 1, in simplifying data manipulation in the recited manner, Applicants respectfully submit that, upon entry of the proposed amendment to claim 1, amended claim 1 and its dependent claims would all be novel and patentably distinct over the prior art of record in this case.

Similar amendment is presented to independent method claim 12 to clarify its patentability over the prior art of record. Proposed amended claim 12 now requires that its writing step contiguously writes, into a most significant portion of a destination operand, non-contiguous data from selected ones of the plurality of fields from the first source operand, and contiguously writes, into a least significant portion of the destination operand, non-contiguous data from selected ones of the plurality of fields from the second source operand that are at the same positions as the selected fields of the first source operand. Support for this proposed amendment is clearly present in the specification,[11] and therefore no new matter is presented by this amendment.

Applicants submit that proposed amended claim 12 and its dependent claims are novel and patentably distinct over the prior art of record in this case.

---

[11] Specification, *supra*, page 26, Table 9; page 30, lines 9 through 12 and lines 17 through 20.

As mentioned above, claim 12 was finally rejected under §102 as anticipated by the Intel reference. The Examiner asserted, relative to the writing step, that the Intel reference teaches the writing of non-contiguous data from selected fields (fields 7, 5, 3, and 1 for the mix1.1 instruction and fields 6, 4, 2, and 0 for the mix1.r instruction) of the first source operand *r2* to a most significant portion of the destination operand *rl* (fields 7, 5, 3, and 1), and the writing of non-contiguous data from selected fields (fields 7, 5, 3, and 1 for the mix1.1 instruction and fields 6,4,2, and 0 for the mix1.r instruction) of the second operand *r3* to a least significant portion of the destination operand *rl* (fields 6, 4, 2, and 0).[12] As discussed above relative to claim 1, the Examiner asserted that the fields 7, 5, 3, and 1 of the destination operand *r1* correspond to a most significant portion of the destination because these fields do not include the least significant field, and that the fields 6, 4, 2, and 0 of the destination operand *r1* correspond to a least significant portion because these fields do not include the most significant field.[13]

As above, Applicants disagree with this interpretation of the reference. Amendment to claim 12 is presented anyway, to advance the prosecution of this case, by clarifying the novelty and inventiveness of this claim even over the Examiner's faulty interpretation of the Intel reference. Claims 15 and 16 are also proposed to be amended, for consistency with the proposed amendment to claim 12, upon which they depend.

Proposed amended claim 12 now requires the contiguous writing of non-contiguous data from selected fields of the first source operand into a most significant portion of the destination operand, and the contiguous writing of non-contiguous data from selected fields of the second source operand, taken from the same positions as those in the first source operand, into a least significant portion of the destination operand. The Intel reference fails to teach this contiguous writing of the non-contiguous data of the respective source operands. Rather, as is clearly shown in the reference,[14] the data from source operands *r2* and *r3* are placed in destination operand in an interleaved fashion relative to one another for both the mix 1.l and

[12] Office Action, *supra*, pages 6 and 7, ¶10(d).
[13] *Id.*
[14] Intel, *supra*, Figure 7-23, page 7-117.

mix 1.r instructions. Upon entry of this amendment, amended claim 12 would therefore be novel over the Intel reference, even if interpreted in the manner presented by the Examiner in the Office Action.

Applicants further respectfully submit that, upon entry of this amendment, claim 12 and its dependent claims would be patentably distinct over the prior art of record in this case.

As mentioned above, the writing step of proposed amended claim 12 is not met by the Intel reference, because the reference fails to disclose the contiguous writing of the non-contiguous data into the destination operand as required by the claim. The Hennessy and Haataja references lack disclosure in this regard, and indeed wholly fail to disclose any byte intermingling operations. Accordingly, the combined teachings of the references fall short of the requirements of proposed amended claim 12.

Applicants further respectfully submit that there is no suggestion from the prior art to modify these teachings in such a manner as to reach the requirements of proposed amended claim 12. This lack of suggestion is apparent from the Intel reference, which presents a wide variation and range of "mix" and "mux" instructions, among others, but apparently sees no need for the byte intermingling required by proposed amended claim 12. The other references, as mentioned above, provide no teachings in this regard. Especially considering the advantages provided by the claimed method in streamlining byte intermingling in a digital system with a microprocessor, Applicants respectfully submit that proposed amended claim 12 and its dependent claims are patentably distinct over the prior art of record in this case.

Claim 7 was finally rejected under §102 as anticipated by the Intel reference. In making the rejection, the Examiner asserted that the reference discloses, relative to its mix 1.l instruction, the placing of the contents of a least significant plurality of fields (*i.e.*, fields 5, 3, and 1) of a second operand *r2* to a least significant portion of a destination operand *rl* (*i.e.*, fields 5, 3, and 1), and the placing of the contents of a most significant plurality of fields (*i.e.*, fields 7, 5, and 3) of a first operand *r0* to a most significant portion of the destination operand

rl (*i.e.*, fields 6, 4, and 2).[15] The Examiner asserted that the most significant portion of the destination register comprises its uppermost seven fields because these fields do not include the least significant field, and that the least significant portion of the destination register comprises is lowermost seven fields because those fields do not include the most significant field.[16]

Again, Applicants disagree with this interpretation of the Intel reference. To advance the prosecution of this case, however, Applicants propose amending claim 7 to clarify its novelty and patentability, over even this erroneous interpretation of the Intel reference.

Proposed amended claim 7 now requires that the byte intermingling circuitry contiguously place the contents of a least significant plurality of contiguous fields selected from the second source operand into a least significant portion of the destination operand, and to also contiguously place the contents of a most significant plurality of contiguous fields selected from the first source operand in a most significant portion of the destination operand. The specification clearly supports this amendment to the claim, for example by way of the example of the PACKHL2 instruction,[17] and as such no new matter is presented by this amendment. As before, proposed amended claim 7 provides important advantages in a digital system, for example by providing single instruction execution techniques for manipulating and preparing pairs of values to be used by packed arithmetic operations.[18]

Applicants respectfully submit that proposed amended claim 7 is not only novel over the Intel reference (even as interpreted by the Examiner), but is also patentably distinct over the prior art of record in this case.

Even accepting, for the sake of argument, the interpretation of the Intel reference posited by the Examiner, the reference nowhere discloses circuitry that contiguously places the contents of a least significant plurality of contiguous fields from one operand into a least significant

---

[15] Office Action, *supra*, pages 3 and 4, ¶9(d).
[16] *Id.*
[17] Specification, *supra*, page 26, Table 9; page 30, lines 13 through 16.
[18] Specification, *supra*, page 26, Table 9.

portion of a destination operand, and that contiguously places the contents of a most significant plurality of contiguous fields from another operand into a most significant portion of the destination operand. Rather, the asserted mix 1.1 instruction of the Intel reference interleaves, into the destination operand, non-contiguous data elements from two source operands.[19] Accordingly, the Intel reference falls short of the requirements of proposed amended claim 7.

Applicants submit that proposed amended claim 7 is not only novel over the Intel reference but is patentably distinct over the prior art of record in this case. None of the other applied references (namely the Hennessy and Haataja references) provide any teachings regarding byte intermingling circuitry that contiguously places the contents of pluralities of contiguous source operand fields in the manner recited by proposed amended claim 7. And there is no suggestion from the prior art to modify these teachings, considering the absence of any byte intermingling teachings in the secondary references, and the wide range of "mix" and "mux" instructions presented by the Intel reference, with no mention of the placing now required by proposed amended claim 7. The advantages of this intermingling for packed arithmetic operations, as mentioned above, support the patentability of these claims as well.

For these reasons, Applicants respectfully submit that, upon entry of this amendment, amended claim 7 will be in condition for allowance.

Claim 17 was also finally rejected as anticipated by the Intel reference. The Examiner asserted that the mix 1.1 instruction met the writing step of the claim, if one considered that the most significant portion of both the operand and destination comprises the upper seven fields (7 through 1) of the destination operand because those fields do not include the least significant field, and considered that the least significant portion of both the operand and the destination comprises the lower seven fields (0 through 6) because those fields do not include the most significant field.[20]

---

[19] Intel, *supra*, Figure 7-23, page 7-117.
[20] Office Action, *supra*, pages 9 and 10, ¶14(c).

Again, Applicants respectfully disagree with this interpretation of the meaning of most and least significant portions of the destination and source operands but, in order to advance the prosecution of this case, propose amending claim 17 to overcome even this strained interpretation of the Intel reference.

Proposed amended claim 17 now requires contiguously writing, into a most significant portion of a destination operand, a most significant plurality of contiguous fields selected from the first source operand, and contiguously writing, into a least significant portion of the destination operand, a least significant plurality of contiguous fields selected from the second source operand. As discussed above relative to claim 7, the specification clearly supports this amendment to the claim,[21] and as such no new matter is presented by this amendment. The method of proposed amended claim 17 enables single instruction execution techniques for manipulating and preparing pairs of values, which are especially beneficial in executing packed arithmetic operations.[22]

Applicants respectfully submit that proposed amended claim 17 is novel over the Intel reference (even as interpreted by the Examiner), and is patentably distinct over it and the other prior art in this case.

Even considering the interpretation of most and least significant portions of the destination operand as presented by the Examiner, the Intel reference nowhere discloses contiguously writing, into a most significant portion of the destination operand, the contents of a most significant plurality of contiguous fields selected from one source operand, and contiguously writing, into a least significant portion of the destination operand, the contents of a least significant plurality of contiguous fields from another operand, as claimed. As discussed above relative to claim 7, the mix 1.1 instruction of the Intel reference instead interleaves non-contiguous data elements from two source operands into the destination operand.[23] The teachings of the Intel reference therefore fails to meet the writing step of proposed amended

---

[21] Specification, *supra*, page 26, Table 9; page 30, lines 13 through 16.
[22] Specification, *supra*, page 26, Table 9.
[23] Intel, *supra*, Figure 7-23, page 7-117.

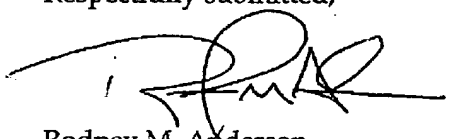
claim 17, and thus falls short of the claim. Proposed amended claim 17 is therefore novel over the Intel reference.

Applicants submit that proposed amended claim 17 is also patentably distinct over the prior art of record in this case. None of the other applied references (namely the Hennessy and Haataja references) provide any teachings concerning the contiguously writing step of proposed amended claim 17, and therefore the combined teachings of the references fall short of the requirements of the claim. In addition, nowhere is there any suggestion from the prior art to modify those combined teachings so as to reach the claim. No such suggestion is present in the Hennessy and Haataja references, as these references are in no way concerned with byte intermingling operations. Despite the numerous variations of "mix" and "mux" instructions disclosed in the Intel reference, there is still no mention of the writing step that is now required by proposed amended claim 17, much less any suggestion to modify these teachings to attain the advantages of this method in byte intermingling for packed arithmetic operations.

For these reasons, Applicants respectfully submit that, upon entry of this amendment, amended claim 17 will be in condition for allowance.

As set forth in these remarks, Applicants respectfully submit that, upon entry of this amendment, all claims in this case will be in condition for allowance. Entry of this amendment, and favorable reconsideration of this application, are therefore respectfully requested.

Respectfully submitted,

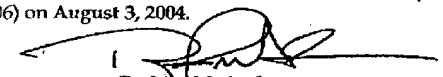


Rodney M. Anderson
Registry No. 31,939
Attorney for Applicants

Anderson, Levine & Lintel, L.L.P.
14785 Preston Road, Suite 650
Dallas, Texas 75254
(972) 664-9554

CERTIFICATE OF FACSIMILE TRANSMISSION
37 C.F.R. 1.8

The undersigned hereby certifies that this correspondence is being facsimile transmitted to the Patent and Trademark Office (Fax Number 703-872-9306) on August 3, 2004.



Rodney M. Anderson
Registry No. 31,939